ABSTRACT

A method of forming floating gate memory cells, and an array formed thereby, wherein each memory cell includes an electrical conductive floating gate having a folded structure over and adjacent to a semiconductor block on a semiconductor substrate. An electrical conductive control gate is formed having a portion disposed over and insulated from the floating gate. Spaced apart source and drain regions are formed self-aligned to source and drain lines with a channel region formed therebetween and along a top and sidewalls of the silicon block. An electrical conductive tunneling gate can be optionally provided over and insulated from the control gate by an insulating layer to form a tri-layer structure permitting both electron and hole charges tunneling through at similar tunneling rate.